All amendments are approved, 3/2/05 JPS

IN THE SPECIFICATION:

Please amend the specification by amending the paragraph from page 19, line 27, to page 20, line 5, as indicated in attached Appendix A.

Please amend the specification by amending the paragraph at page 20, lines 17-23, as indicated in attached Appendix B.

Please amend the specification by amending the paragraph at page 31, lines 15-17, as indicated in attached Appendix C.

Please amend the specification by amending the paragraph at page 32, lines 14-23, as indicated in attached Appendix D.

Please amend the specification by amending the paragraph from page 27, line 28, to page 28, line 5, as indicated in attached Appendix E.

Please amend the specification by amending the paragraph at page 34, lines 1-14, as indicated in attached Appendix F.

Please amend the specification by amending the paragraph at page 37, lines 4-9, as indicated in attached Appendix G.

Please amend the specification by amending the paragraph at page 42, lines 16-23, as indicated in attached Appendix H.

Please amend the specification by amending the paragraph from page 42, line 24, to page 43, line 2, as indicated in attached Appendix I.

Please amend the specification by amending the paragraph at page 43, lines 3-9, as indicated in attached Appendix J.

Please amend the specification by amending the paragraph at page 43, lines 10-16, as indicated in attached Appendix K.

Please amend the specification by adding a paragraph at page 15, between lines 26 and 27, as indicated in attached Appendix L.

IN THE ABSTRACT:

Please amend the abstract at page 70, lines 3-21, as indicated in attached Appendix M.

IN THE CLAIMS:

Please amend claims 23 and 49 as indicated in attached Appendix N.

Please add claims 89-93 as indicated in attached Appendix N.

A listing of the status of all claims 1-93 in the present patent application is provided in attached Appendix N.

Approved 3/2/05 JJG

APPENDIX M

A method and apparatus for evaluating and optimizing a signaling system is described. ~~Evaluation is accomplished using the same circuits actually involved in normal operation of the signaling system. Capability for in situ testing of a signaling system is provided, and information may be obtained from the actual perspective of a receive circuit in the system.~~ A pattern of test information is generated in a transmit circuit of the system and is transmitted to a receive circuit. A similar pattern of information is generated in the receive circuit and used as a reference. The receive circuit compares the patterns. Any differences between the patterns are observable. ~~Preferably, the patterns are repeating patterns that allow many iterations of testing to be performed.~~ In one embodiment, a linear feedback shift register (LFSR) is implemented to produce patterns. ~~Information obtained from testing may be used to assess the effects of various system parameters, including but not limited to output current, crosstalk cancellation coefficients, and self equalization coefficients, and system parameters may be adjusted to optimize system performance.~~ An embodiment of the invention may be practiced with various types of signaling systems, including those with single-ended signals and those with differential signals. An embodiment of the invention may be applied to systems communicating a single bit of information on a single conductor at a given time and to systems communicating multiple bits of information on a single conductor simultaneously.

Approved 3/2/05 JAJ

APPENDIX L

At this point it should be noted that the transmit repeating pattern may be received in a test receiver (not shown) separate from the receive circuit 103 when the transmit circuit 101 is operating in a test mode. Also, the transmit repeating pattern may be transmitted from a test transmitter (not shown) separate from the transmit circuit 101 when the receive circuit 103 is operating in a test mode.

Approved 3/2/05 BJ

APPENDIX K

A fixed logic zero signal is coupled at node 852 to an input of a shift register comprising flip-flops 866, 868, 870, and 872. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 854. A transmit clock signal is provided to a clock input of the shift register at node 856. Nodes 858, 860, 862, and 864 are coupled to parallel load data inputs of flip-flops 866, 868, 870, and 872, respectively. A serial data output of the shift register at the output of flip-flop 872 is coupled to an input of multiplexer 876 at node 874.

Approved 3/2/05 MB

APPENDIX J

A fixed logic zero signal is coupled at node 851 to an input of a shift register comprising flip-flops 865, 867, 869, and 871. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 853. A transmit clock signal is provided to a clock input of the shift register at node 855. Nodes 857, 859, 861, and 863 are coupled to parallel load data inputs of flip-flops 865, 867, 869, and 871, respectively. A serial data output of the shift register at the output of flip-flop 871 is coupled to an input of multiplexer 876 at node 873.

Approved 3/2/05 MF

APPENDIX I

A fixed logic zero signal is coupled at node 802 to an input of a shift register comprising flip-flops 816, 818, 820, and 822. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 804. A transmit clock signal is provided to a clock input of the shift register at node 806. Nodes 808, 810, 812, and 814 are coupled to parallel load data inputs of flip-flops 816, 818, 820, and 822, respectively. A serial data output of the shift register at the output of flip-flop 822 is coupled to an input of multiplexer 826 at node 824.

Approved 3/2/05 JPL

APPENDIX H

Figure 8 is a logic diagram illustrating a prior art quad signaling level transmit circuit. A fixed logic zero signal is coupled at node 801 to an input of a shift register comprising flip-flops 815, 817, 819, and 821. A load signal for performing a parallel data load of the shift register is provided to the shift register at node 803. A transmit clock signal is provided to a clock input of the shift register at node 805. Nodes 807, 809, 811, and 813 are coupled to parallel load data inputs of flip-flops 815, 817, 819, and 821, respectively. A serial data output of the shift register at the output of flip-flop 821 is coupled to an input of multiplexer 826 at node 823.

Approved 3/2/05

APPENDIX G

An output of ~~even~~ odd receiver 306 at node 308 is coupled to an input of a shift register comprising flip-flops 314, 316, 318, and 320. A receive clock is provided to a clock input of the shift register at node 310. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 312. Parallel data are provided at parallel data outputs 322, 324, 326, and 328 of flip-flops 314, 316, 318, and 320, respectively.

Approved 3/2/05 MK

APPENDIX F

The method of Figure 32 may be performed until the system reaches a generally steady state condition. Such steady state conditions may be defined at a plurality of levels. For example, at a broader level, the steady state condition may be more approximate, while, at a narrower level, the steady state condition may be more precise. As an example, a steady state condition may be identified when step 3209 ~~is~~ occurs, especially if it occurs several times over a relatively small range of adjustment of the relevant system parameter. Adjustment back and forth within a limited range may be observed as "dithering" and may be used to indicate completion of the method of Figure 32. If hysteresis occurs during adjustment, such that no specific value for the system parameter is identified for the steady state condition, a value can be interpolated within the range of adjustment observed. For example, a value in the middle of the range may be selected. When the method of Figure 32 is completed for one system parameter, it may be repeated for a different system parameter. Alternatively, multiple system parameters may be adjusted simultaneously.

Approved 3/7/05 JPL

APPENDIX E

Evaluation of a signaling system may be performed at ~~a~~ many different times. For example, evaluation may performed during a manufacturing process, at system start-up, when a communication failure is detected, or during normal operation of a signaling system. Evaluation may be performed occasionally between periods of communication of user data between the transmit circuit and the receive circuit. As an example of evaluation at system start-up, evaluation may be performed before the system is operating normally and ready to communicate user data.

Approved TRS 3/2/05

APPENDIX D

Receiver circuit 3103 comprises receiver 3116, multiplexer 3119, shift register 3108, and XOR gate 3113. Medium 3102 is coupled to an input of receiver 3116. A receive circuit timing signal is coupled to an input of receiver 3116 at node 3117. A voltage reference signal is coupled to an input of receiver 3116 at node 3118. An output of receiver 3116 is coupled to an input of multiplexer 3119 and to an input of XOR gate 3113. A fill pipe signal is coupled to a selection input of multiplexer 3119 at node 3120. An output of multiplexer 3119 is coupled to a serial data input of shift register 3108. A serial data output of shift register 3108 is coupled to an input of multiplexer 3119 and to an input of XOR gate 3113 via line 3111. An output of XOR gate 3113 provides an error output at node 3114.

Approved 3/2/05 JSH

APPENDIX C

The example of Figure 28 illustrates samples of waveforms exhibiting the effects of crosstalk induced by other nearby conductors, as can be seen, for example at locations 2801, 2802, 28053, and 2804.

Approved 3/2/05 PS

APPENDIX B

Figure 20 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 2001 at a gate of a first input transistor 2003 and to an input 2002 at a gate of a second input transistor 2004. A source of the first input transistor 2003 and a source of the second input transistor 2004 are coupled to a first terminal 2011~~9~~ of current source 2012~~0~~. A second terminal 20~~2~~13 of current source 2012~~0~~ is coupled to ground.

Approved 3/2/05 JBL

APPENDIX A

Figure 19 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 1901 at a gate of a first input transistor 1903 and to an input 1902 at a gate of a second input transistor 1904. A source of the first input transistor 1903 and a source of the second input transistor 1904 are coupled to a first terminal 1911~~9~~ of current source 1912~~0~~. A second terminal 19~~2~~13 of current source 1912~~0~~ is coupled to ground.